Design, modelling, and test of a solid-state main breaker for hybrid DC circuit breaker

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«DC circuit breaker», «IGBT», «Medium voltage DC-grid», «Parallel operation», «Protection device»

Abstract

Driven by the requirements of reducing air pollutant gas emissions and fuel consumption, the concepts of more electric ship and electric aircraft are attracting increasing attention. Medium voltage DC (MVDC) distribution architectures have been proposed as potential candidates to transmit and distribute energy from generators to motors in these applications. However, the low impedance in MVDC systems results in extremely fast propagation speed of fault currents. Therefore, it is necessary to interrupt the DC fault in a very short period. This paper investigates a solid-state circuit breaker with an ultrafast interruption speed as a main breaker for a hybrid DC circuit breaker. A simulation model of the hybrid circuit breaker is established using PLECS software to evaluate the performance of the main breaker. A 1 kV solid-state main breaker prototype based on series and parallel connected insulated gate bipolar transistors (IGBTs) is built. Series and parallel connection of IGBTs are implemented to increase the voltage and current level. The maximum voltage across the solid-state circuit breaker is limited to 1.8 kV during current interruption. The solid-state main breaker prototype is experimentally tested under dynamic current conditions. The solid-state main breaker prototype successfully interrupts current of 400 A within 300 microseconds and presents good voltage balancing as well as current sharing performance. The experimental results show good agreement with the simulation results.

Introduction

More electric ship and electric aircraft have attracted a lot of research interest in recent years due to their higher energy efficiency, lower environmental impact, fewer fuel burns and reduced weight. Medium voltage direct current (MVDC) system has been proposed as a potential solution to ensure a high reliability and high quality power supply for electric ship [1, 2] and turboelectric aircraft [3, 4]. However, because of the high rate of rise of the fault current and the absence of natural current zero-crossing in the DC system, the design of DC circuit breakers is more challenging than that of AC circuit breakers [5, 6]. Moreover, the fault current propagates at extremely fast speed as the DC system has low impedance. It is critical to isolate a DC fault in a very short time (within a few milliseconds). Therefore, DC circuit breakers with ultrafast interruption speed are the key enabling technology and indispensable to achieve the multi-terminal DC (MTDC) system.

There are three types of DC circuit breakers: mechanical circuit breaker (MCB), solid-state circuit breaker (SSCB), and hybrid circuit breaker (HCB) [7]. MCB has negligible on-state loss, tens-of-milliseconds interruption time is unacceptable in DC system. In contrast, SSCB can achieve ultrafast interruption speed in a few hundred microseconds. However, the on-state loss is high, which reduces the system efficiency. Xi'an Jiaotong University developed and investigated a 10 kV SSCB based on series connected press-pack insulated gate bipolar transistors (IGBTs), which successfully interrupted 5.1 kA within 1 ms [8]. Hybrid DC circuit breaker is a combination of mechanical switch and solid-state

semiconductor switch, which is proposed to realize fast operation as well as low on-state loss. An HCB has lower on-state losses than SSCB and can achieve faster interruption than MCB.

A proactive hybrid DC circuit breaker concept has been proposed by ABB in 2012, as shown in Fig. 1, which is the first HCB for high voltage DC system [9]. The proactive HCB consists of a mechanical branch, a semiconductor branch and an energy absorption branch. The current normally flows through the mechanical branch, which combines a mechanical switch (MS) with a load commutation switch (LCS). The power electronic devices in the semiconductor branch act as the main breaker (MB). The energy absorption branch is made up of metal oxide varistors (MOVs) to limit the voltage across the circuit breaker during interruption and absorb any residual energy in the system inductance. An 80 kV main breaker cell has been developed by ABB based on series connection of IGBTs, which can interrupt 9 kA within 5 ms.

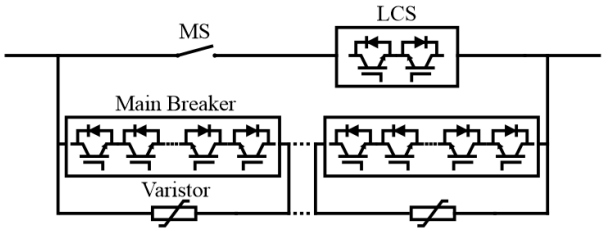


Fig. 1: Proactive hybrid circuit breaker proposed by ABB

Global Energy Interconnection Research Institute (GEIRI) has developed a ± 200 kV HCB using IGBT-based H-bridge as the main breaker for Zhoushan five-terminal HVDC project, which can break 15 kA within 3 ms [10, 11]. NR Electric Co., Ltd. has built a ± 535 kV HCB for Zhangbei four-terminal HVDC project, which is the first HVDC circuit breaker for 500 kV level. This HCB uses IGBTs in diode-based H-bridge as the main breaker and series connected IGBTs as LCS [12]. GEIRI has also developed a ± 535 kV HCB for Zhangbei project, which applies diode-based H-bridge modules as the main breaker and IGBT-based H-bridge modules as LCS [13]. Beside the design for high voltage DC system, North Carolina State University has designed a 10 kV HCB for medium voltage level. The HCB uses a 15 kV silicon carbide (SiC) emitter turn-off (ETO) thyristor in diode-based H-bridge as the main breaker. This medium voltage HCB has demonstrated a successful interruption of 100 A within 2 ms [14, 15].

Series and parallel connection of semiconductors are required to increase the voltage and current level of the solid-state main breaker. The performance of the solid-state main breaker using both series and parallel connection of IGBTs has not been discussed in detail in previous research. In this paper a 1 kV solid-state main breaker prototype based on series and parallel connected IGBTs is simulated, built and experimentally tested under fault interruption conditions. The use of series and parallel connection of IGBTs to increase the voltage and current level of the solid-state main breaker is important. The current sharing in the parallel branches and the voltage balancing in the series connection must be investigated. The operation of the solid-state main breaker in a hybrid circuit breaker is simulated in PLECS software. The voltage balancing and current sharing performance during dynamic condition are investigated through both simulation and experimental testing.

Proposed solid-state DC main breaker

Fig. 2 presents the topology of the proposed solid-state DC circuit breaker as the main breaker in the hybrid DC circuit breaker, which consists of two IGBT modules connected in parallel. Each module has two IGBTs in series and each IGBT has an anti-parallel body diode. The current sharing between parallel connected IGBTs and voltage balancing between series connected IGBTs are investigated using this topology. Balancing resistor R_s is utilized for static voltage balancing at the off state of IGBT and resistor-capacitor-diode (RCD) snubber circuit is selected for dynamic voltage balancing during current interruption [16]. Three metal-oxide varistors (MOVs) are used in the proposed solid-state main breaker to absorb the residual energy in the system. The varistor MOV1 limits the maximum voltage across the

solid-state main breaker during current interruption and the varistor MOV2 and MOV3 protect individual IGBT in case the voltage is unbalanced.

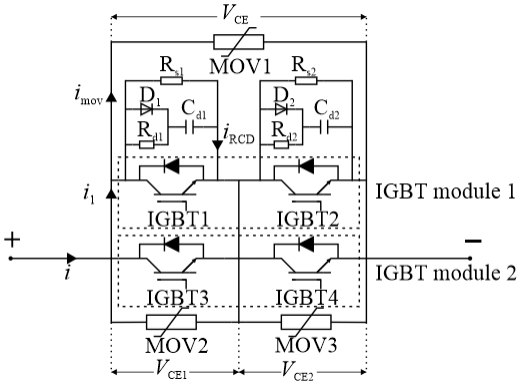


Fig. 2: Topology of the proposed solid-state main breaker

Simulation of hybrid circuit breaker

A simulation model is established in PLECS software to simulate the performance of the solid-state DC circuit breaker as the main breaker in the hybrid circuit breaker. As shown in Fig. 3, the hybrid circuit breaker is placed in a test circuit. The test circuit is an LC resonant circuit which can emulate the rising of the fault current in the DC system. The topology of the solid-state main breaker is the same as in Fig. 2. An ideal switch acts as the MS and a MOSFET is applied as the LCS in the mechanical branch. The parameters of simulation model are listed in Table II.

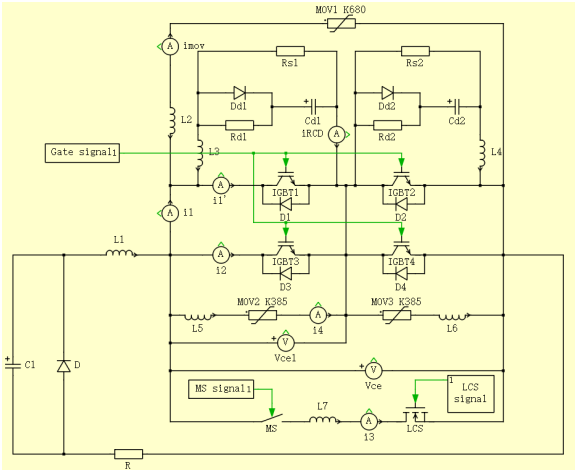


Fig. 3: Simulation of hybrid circuit breaker

Table II: Component parameters of the simulation model

Parameter	Value	Parameter	Value
DC capacitor C1	12 mF	Static balancing resistor Rs1, Rs2	20 kΩ
Line inductor L1	1 mH	Snubber resistor Rd1, Rd2	30 Ω
Line resistor R	55 mΩ	Snubber capacitor Cd1, Cd2	6 µF
Estimated stray inductance associated with MOVs L2, L5, L6	1 µH	Estimated stray inductance associated with RCD L3, L4	2 µH
Estimated stray inductance associated with mechanical branch L7	6 µH		

The interruption process of the hybrid circuit breaker is illustrated in Fig. 4. The voltage across the circuit breaker V_{CE} and voltage across one IGBT V_{CE1} are monitored. i_1', i_2 and i_3 represent the currents flowing through the IGBT module 1 branch, IGBT module 2 branch, and mechanical branch, respectively. At the beginning of the simulation, the MS and LCS are closed and the solid-state main breaker is open. The fault current i is generated by discharging the capacitor C1, and the rising rate of the fault current is limited by the line inductance L1. The fault current only flows through the mechanical branch. When the fault is detected at 2 ms, the solid-state main breaker is closed and the LCS is open. The fault current commutates from the mechanical branch (i_3) to the main breaker branch (i_1'+ i_2). After the fault current fully transfers to the main breaker branch, the MS can be separated without arcing. In Fig. 6, the MS is simulated to be opened at 4 ms. When the current flows through the main breaker branch (from 2 ms to 5 ms), the current in two IGBT branches (i_1'+ i_2) is twice as much as that in one IGBT branch (i_1'). Therefore, the current is shared evenly between two IGBT branches. The fault current reaches to 400 A at 5 ms, at which time four IGBTs are turned off. The voltage V_{CE} is clamped by the varistor MOV1, which is twice the value of V_{CE1}. The main breaker exhibits perfect voltage balancing during interruption.

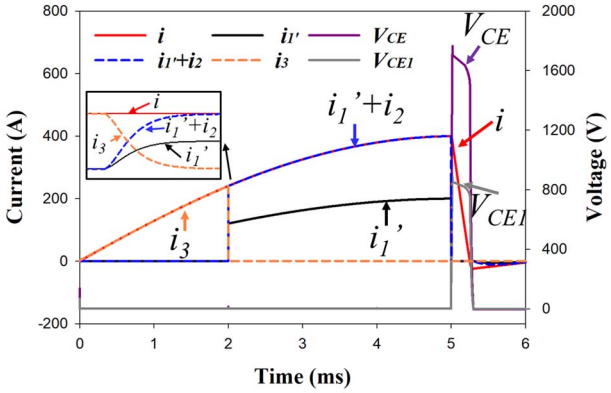


Fig. 4: Simulation of interruption process of hybrid circuit breaker of 400 A peak current value

Fig. 5 presents three currents (i, i_{MOV}, and i_{RCD}) and the voltage across the hybrid circuit breaker V_{CE} during the interruption process of the solid-state main breaker at around 5 ms. i_{MOV}, and i_{RCD} denote the currents flowing through the MOV1 branch and the RCD snubber circuit, respectively. In Fig.7(a), the IGBTs are turned off at 5 ms, the fault current is commutated to the RCD snubber circuit. The snubber capacitors are charged until V_{CE} reaches the clamping voltage of the MOV1. At the same time, the current transfers from the RCD snubber circuit to the MOV branch. And then, the fault current i gradually decreases and drops to zero at around 5.25 ms because the MOV voltage is higher than the DC system voltage. The solid-state main breaker can interrupt a 400 A DC current within 250 µs. Fig.7(b) presents interruption process from 4.98 ms to 5.05 ms in the details. It should be pointed out that there is a voltage spike of 900 V in Fig. 5(b), which is caused by the stray inductance associated with the snubber circuit and the IGBTs.

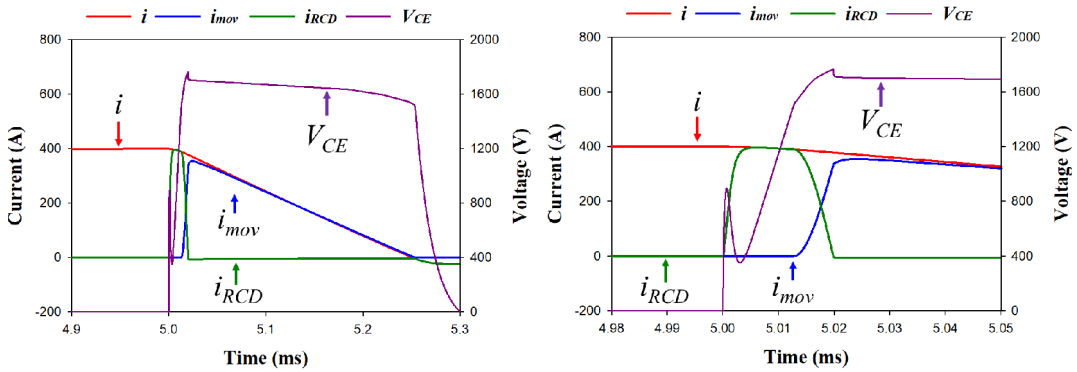


Fig. 5: Simulation result of interruption of 400 A: (a) current commutation from IGBT to RCD and MOV; (b) zoom in for (a)

Design of solid-state main breaker

Device selection

Fig. 6 illustrates an equivalent circuit of DC system with solid-state main breaker during a fault. When the solid-state main breaker is in on state, almost all the equivalent DC system voltage V_{DC} is applied on the system inductor which causes a rapid increase in fault current.

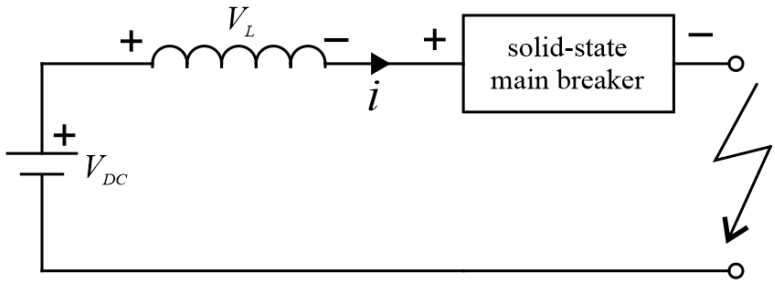


Fig. 6: Solid-state main breaker in the equivalent DC system circuit

When the fault current is detected, the solid-state main breaker starts to interrupt the current. All IGBTs are turned off simultaneously, the fault current commutates from IGBTs to the RCD snubber circuit in few microseconds and the voltage across the solid-state main breaker increases. After tens of microseconds, the voltage is clamped to a designed level, and the fault current commutates to the varistor. The voltage across the solid-state main breaker is limited by the clamping voltage ($V_{clamping}$) of the MOV1. The clamping voltage should be higher than the DC system voltage, therefore, the negative voltage applied to the inductor can reduce the fault current. All residual energy will be dissipated through the varistor. The current in the circuit can be calculated as follows:

$$i = i_0 - \frac{V_{clamping} - V_{DC}}{L} t \tag{1}$$

where i_0 is the maximum fault current flows through the varistor MOV1, and L is the total inductance in the system. The period that current flows through the varistor is:

$$T = \frac{L \times i_0}{V_{clamping} - V_{DC}} \tag{2}$$

The total energy dissipated by the varistor can be calculated by:

$$W_{total} = \int_0^T V_{clamping} \times i \, dt = \frac{1}{2} L {i_0}^2 \times \left(\frac{V_{DC}}{V_{clamping} - V_{DC}} + 1 \right) \tag{3}$$

High clamping voltage can reduce the interruption time and reduce the total dissipation energy of the varistor. However, the circuit breaker has to withstand the clamping voltage during interruption.

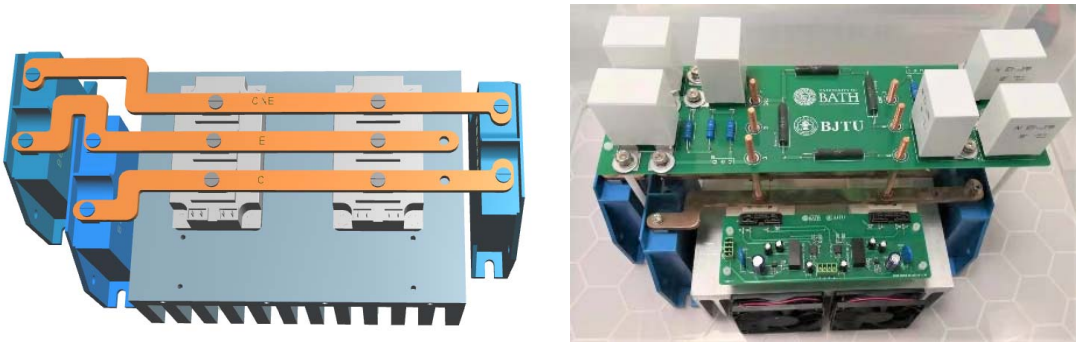
In this paper, IGBT module FF450R12KT4 from Infineon is selected for the 1 kV solid-state main breaker prototype. The IGBT module has two 1.2 kV IGBTs in series, which is more compact and convenient for connecting two IGBT modules in parallel to increase current carrying capability. The maximum voltage across the solid-state main breaker will be suppressed to 1.8 kV by varistor. In addition, varistor MOV2 and MOV3 are employed to limit the maximum voltage to 1 kV to protect IGBTs. Table I lists the devices selected for the solid-state main breaker.

Table I: Devices for the solid-state main breaker

Item	Manufacture	Product
IGBT module 1 & 2	Infineon	FF450R12KT4
MOV1	EPCOS TDK	B80K680
MOV2 & MOV3	EPCOS TDK	B80K385

Mechanical structure

Fig. 7 presents the 3D design and photo of the proposed solid-state main breaker. Two IGBT modules are assembled on a heatsink and connected in parallel using copper bars. MOVs are connected to the copper bars at both sides of the heatsink. The static and dynamic voltage balancing circuits are assembled on the top of the IGBT modules and the gate drive circuit is placed close to the IGBT modules.



(a) (b)

Fig. 7: Mechanical structure of the proposed topology: (a) 3D design; (b) photo of the prototype

DC fault current test

Test platform

The schematic diagram of DC fault current test circuit is presented in Fig. 8. An LC resonant circuit is used in the test circuit to emulate the rising of the fault current in the DC system. The DC fault current test circuit is designed to achieve maximum current at 5.5 milliseconds. Two 6 mF capacitors are connected in parallel and an air core inductor of 1 mH is designed. The capacitors are pre-charged by a DC power supply. The freewheeling diode is used to protect the capacitor from the reverse voltage.

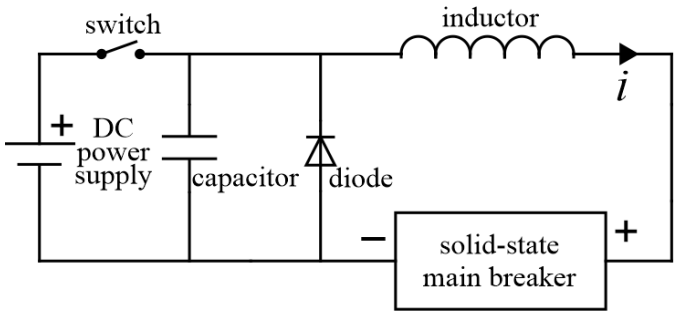


Fig. 8: Schematic diagram of DC fault test circuit

Fig. 9 shows the DC fault test circuit and the solid-state main breaker under test. A microcontroller on the control board is programmed to control the gate drive circuit to provide synchronous gate drive signals for the four IGBTs. The oscilloscope is used to display and record currents (i, i_1, i_{MOV}, and i_{RCD}) and voltages (V_{CE} and V_{CE1}) as illustrated in Fig. 2.

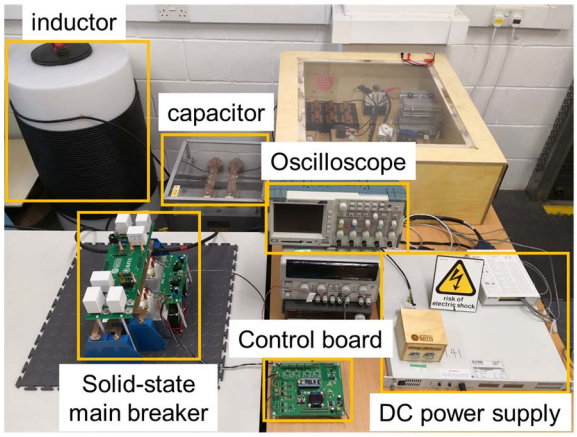


Fig. 9: Dynamic test platform

Current commutation test

In the hybrid DC circuit breaker, the current flows through the MS and LCS (mechanical branch) during normal operation. Once a fault is detected, the current is commutated to the IGBT branches of the solid-state main breaker. The test aims to investigate the current and voltage behaviors during the current commutation from the mechanical branch to solid-state main breaker. During the current commutation tests, the fault current flows through the solid-state main breaker with peak current from 25 A to 400 A. The capacitor, as shown in Fig. 8, is pre-charged to a specific level and the solid-state main breaker is turned on at 5 ms to trigger the LC resonant circuit. The total fault current i, IGBT module 1 current i_1, the total voltage drop V_{CE} and single IGBT voltage drop V_{CE1} are recorded in this test. Because almost no current flows through varistor MOV1 and snubber circuit during the current commutation test, the current i_1 represents the current flowing through IGBT module 1. Fig. 10 shows the current commutation test results when the peak current is 400A. It can be seen that the total current i is approximately twice as much as IGBT module 1 current i_1, which means that the current is evenly shared between parallel IGBT modules. Moreover, in the off state, the total voltage drop across the solid-state main breaker is about twice the voltage drop across one IGBT. Therefore, the solid-state main breaker presents a good static voltage balancing in the off state.

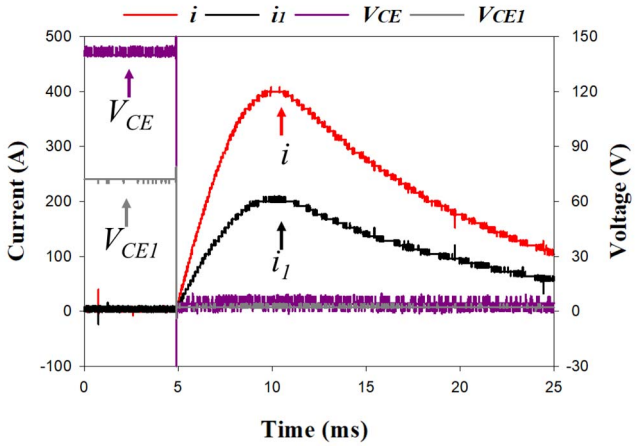


Fig. 10: Current commutation test with peak current of 400A

Current interruption test

The current interruption of the proposed solid-state circuit breaker needs to be investigated because it acts as the main breaker to interrupt the fault DC current in an HCB. The capacitor in Fig. 8 is pre-charged to a specific level, and the voltage level is increased step by step to generate different prospective fault currents. The microcontroller is programmed to turn on the solid-state main breaker to initiate the test and subsequently turn off at 5 ms, at which time the current is close to the peak fault current. Fig. 11 and Fig. 12 show the currents and voltages when the solid-state main breaker interrupts a fault current at 400 A.

Fig. 11(a) illustrates the dynamic current sharing and voltage balancing from fault ignition to current interruption. It should be noted that as shown in Fig. 2, i_1 measures the sum of the current flowing through IGBT branch 1, RCD snubber circuit, and MOV1 branch. i_1 denotes the current flowing through IGBT branch 1 before IGBTs turned off, after they turned off, i_1 represents the current in snubber circuit and MOV1. As shown in Fig. 11(a), the solid-state main breaker is turned on to initiate the test, the total fault current increases from 0 A to 400 A in 5 ms. During this period, the total current i is twice the current in IGBT1, which shows that the IGBT branches share the current evenly under dynamic current change.

Fig. 11(b) highlights the dynamic current sharing and voltage balancing during current interruption. When the IGBTs are turned off, the current commutates to RCD snubber circuit and then to MOV1, the voltage across the solid-state main breaker V_{CE} is approximately twice that of the voltage across one IGBT V_{CE1}. The solid-state main breaker presents good dynamic voltage balancing during the current interruption. When the IGBTs are turned off, the fault current i and i_1 are the same because the current flowing through IGBT branches are zero. The fault current finally reduces to zero within 300 μs.

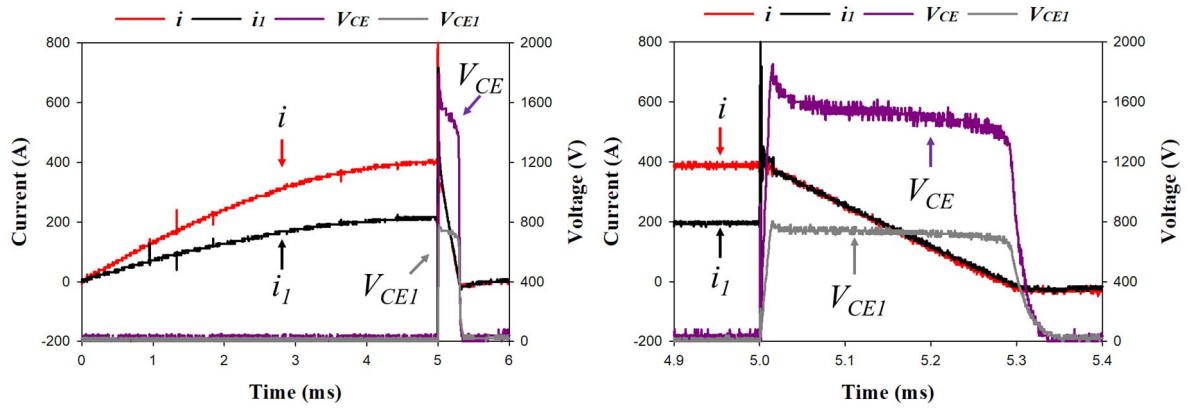


Fig. 11: Current interruption test of 400 A: (a) current share and voltage balance waveform; (b) zoom in for (a)

Fig. 12 presents the current commutation and interruption process of the solid-state main breaker. Three currents (i, i_{MOV}, and i_{RCD}) and the voltage V_{CE} are presented. The fault current i commutates to the RCD snubber circuits once the IGBTs are turned off. The current i_{RCD} flows through the diode and charges the snubber capacitors. After several tens of microseconds, the voltage V_{CE} reaches the knee point of the MOV1, the fault current i then commutates from RCD snubber circuits to the varistor MOV1 branch in several microseconds. The fault current finally reduces to zero within 300 microseconds. The experimental test results show good consistent with simulation results in Fig. 5.

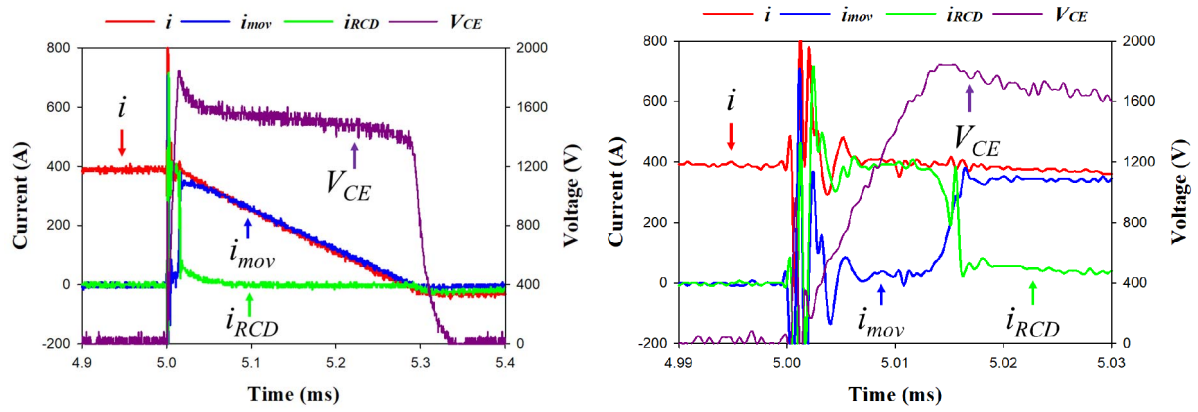


Fig. 12: Current interruption test of 400 A: (a) current commutation from IGBT to RCD and MOV; (b) zoom in for (a)

Conclusions

The performance of the solid-state main breaker in the hybrid circuit breaker is simulated in the PLECS model. A 1 kV solid-state main breaker prototype based on series and parallel connected IGBTs is designed and built. The solid-state main breaker prototype is experimentally tested under dynamic operation using the DC fault test platform. The experimental results show good consistency with the simulation results. The solid-state main breaker prototype successfully interrupts 400 A DC current within 300 μs (including the time to absorb the residual energy). The prototype demonstrates even current sharing under dynamic current change and voltage balancing under both off state and current interruption.

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